

FIG. 1A

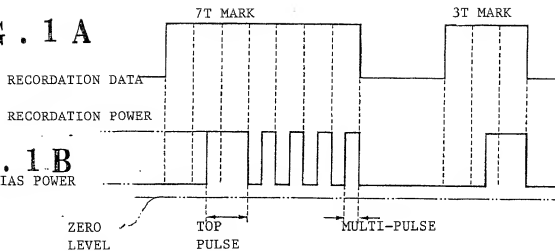


FIG. 1B

BIAS POWER

FIG. 2A

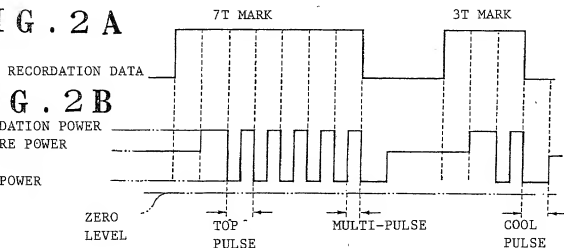


FIG. 2B

RECORDATION POWER
ERASURE POWER

BIAS POWER

FIG. 3A

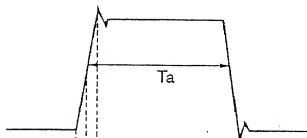


FIG. 3B

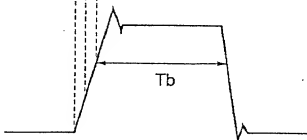


FIG. 4A

WRITE PULSE

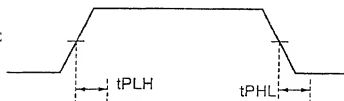


FIG. 4B

IN PHASE OUTPUT

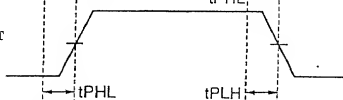
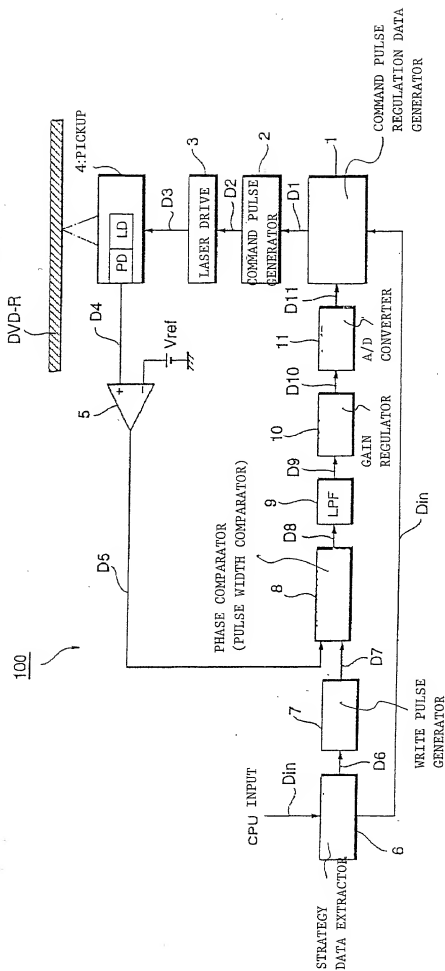


FIG. 4C

INVERTED OUTPUT



FIG. 5



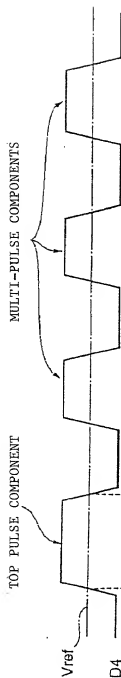


FIG. 6A

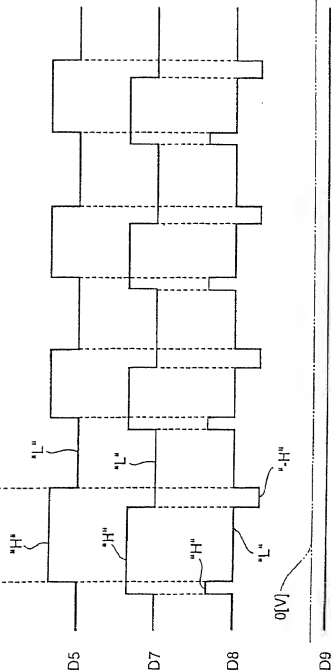


FIG. 6B

FIG. 6C

FIG. 6D

FIG. 6E

TIME

FIG. 7 A

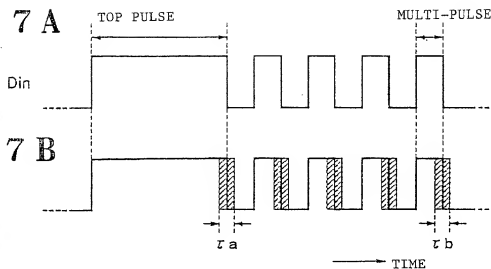


FIG. 7 B

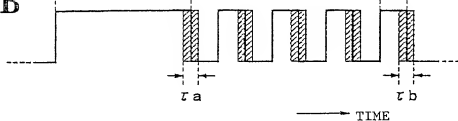


FIG. 8



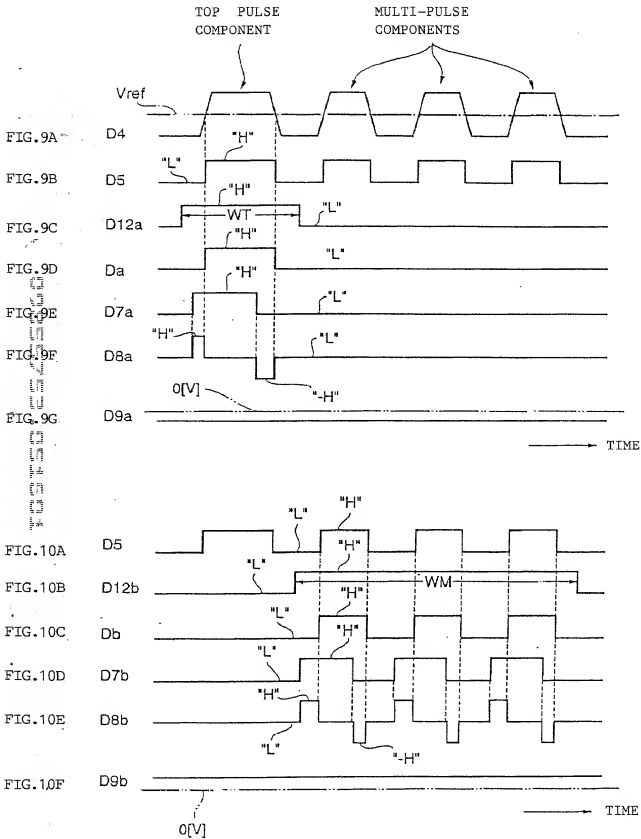
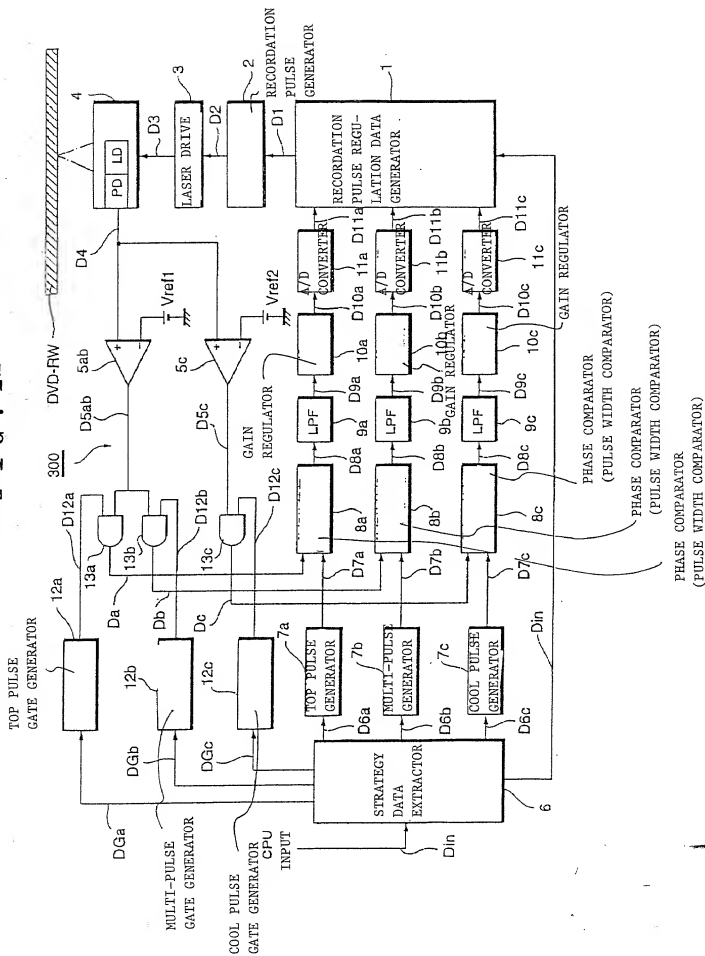


FIG. II



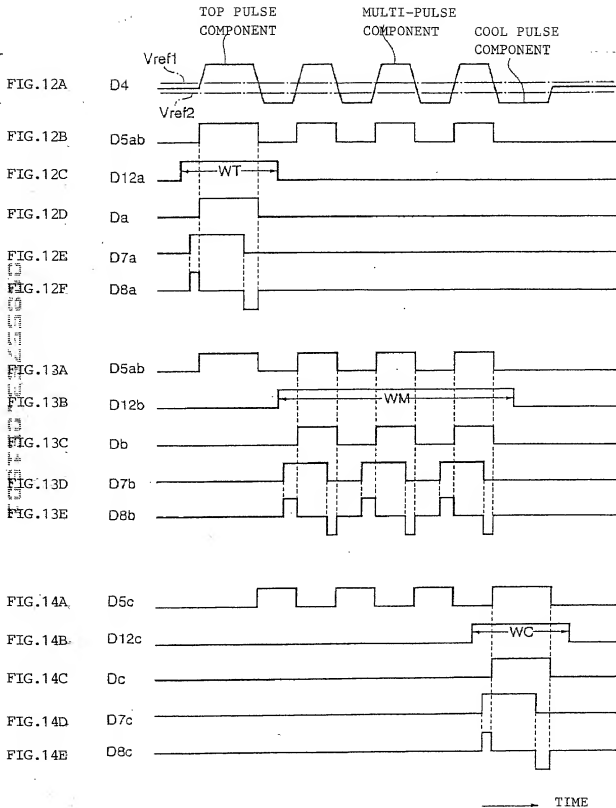
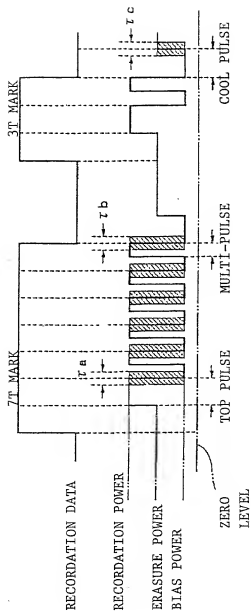


FIG.15A

FIG.15B



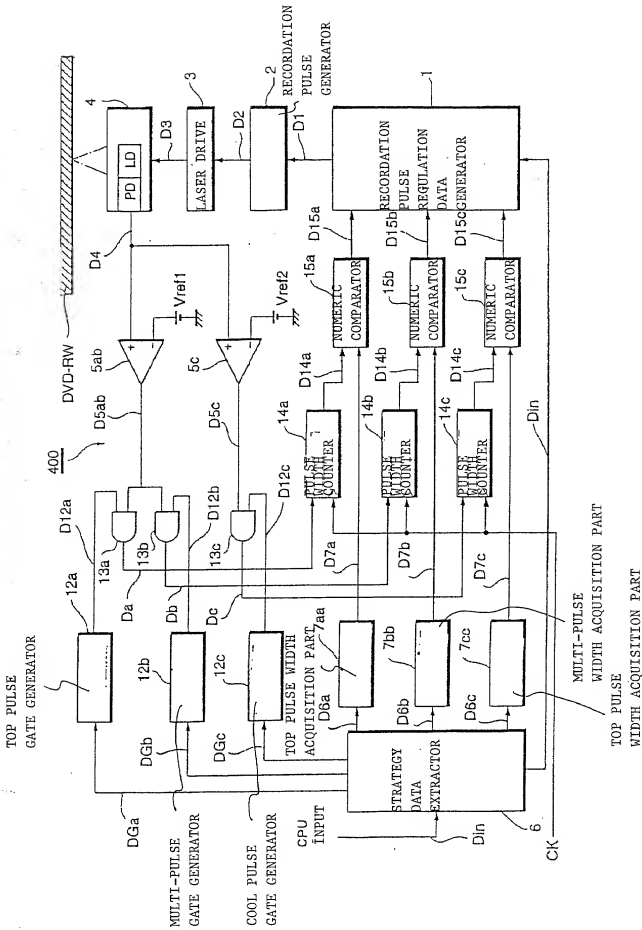


FIG. 16